functionality. Whether such functionality can be implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium can be coupled to the processor such the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. For example, although the description specifies that the radio access network 20 can be implemented using the Universal Terrestrial Radio Access Network (UTRAN) air interface, alternatively, in a GSM/GPRS system, the access network 20 could be a GSM/EDGE Radio Access Network (GERAN), or in an inter-system case it could be comprise cells of a UTRAN air interface and cells of a GSM/EDGE air interface. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. A method of communicating information over a channel, comprising:

framing, above a radio link control layer, rows of a first-type of information comprising payload data in a first format over a radio bearer from a first source to generate rows of a second type of information;

encoding, above the radio link control layer, rows of the second-type of information to generate rows of redundancy information comprising parity blocks;

appending the rows of redundancy information to the rows of second-type information to produce an outer code block that comprises rows of the payload data in the second format and the parity blocks;

adding overhead information to each row of the outer code block, wherein the overhead information includes a sequence number; and

transmitting the outer code block to the radio link control layer.

2. A method according to claim 1, further comprising:

receiving the outer code block from the first source.

3. A method according to claim 2, further comprising:

receiving a second packet from a second source that is identical to the rows of second type information when a wireless communicator undergoes a transition; and

using the sequence number to realign the outer code block with the second packet.

4. A method according to claim 1, wherein the second-type of information comprises payload data in a second format and in some cases padding information.

5. A method according to claim 1, wherein the sequence number provided before encoding allows the radio link controller to change modes when a wireless communicator undergoes a transition.

6. A method according to claim 1;

wherein the encoding comprises outer encoding and is performed independent of the radio link control layer.

7. A method according to claim 1, wherein the channel is a unidirectional, common logical channel.

8. A method according to claim 7, wherein the channel is a unidirectional downlink channel.

9. A method according to claim 7:

wherein the common logical channel carries information that is broadcast to one or more terminals.

10. A method of transmitting a first outer code block and a second outer code block to a wireless communicator, comprising:

transmitting the first block, wherein the first block has at least one data row and at least one redundancy row generated above a radio link control layer, and wherein the each row has a overhead information that includes a sequence number, wherein the second block consists of only data rows; and

when the wireless communicator undergoes a transition, using the sequence number to align the first block with the second block.

11. A communication method using a protocol structure for a communication system, comprising a radio link control layer and a forward error correction layer disposed above the radio link control layer, the method comprising:

receiving by the forward error correction layer a first-type of information over a radio bearer before the first-type of information reaches the radio link control layer;

framing by the forward error correction layer the first-type of information into equal size frames before the first-type of information reaches the radio link control layer to generate a second-type of information;

using the second-type of information in the forward error correction layer to generate rows of redundancy information that are added to the second-type of information to generate an outer code block; and